CLAIMS

1. A timing adjusting method characterized by the fact that in a timing adjusting method for adjusting the timing of an event, said timing adjustment of said event is performed based on multiphase clocks.

2. The timing adjustment method described in Claim 1 characterized by the fact that said event is an electrical event.

3. The timing adjustment method described in Claim 2 characterized by the fact that said electrical event refers to at least one transition that takes place between plural electrical states.

4. The timing adjustment method described in Claim 3 characterized by the fact that said transition between electrical states rises or falls at prescribed pulses.

5. The timing adjustment method described in Claim 4 characterized by the fact that said multiphase clocks are generated from a reference signal pertaining to said prescribed pulses.

6. The timing adjustment method described in Claim 5 characterized by the fact that one selection from said multiphase clocks is used in forming said rise or fall of said prescribed pulses.

7. The timing adjustment method described in Claim 3 characterized by the fact that said transition between electrical states is a transition in digital transmission data.

8. The timing adjustment method described in Claim 7 characterized by the fact that said multiphase clocks are generated from the transmission clock of said digital transmission data.

9. The timing adjustment method described in Claim 8 characterized by the fact that one selection from said multiphase clocks is used in forming a transition after timing adjustment in said digital transmission data.

10. A timing adjustment method characterized by the following facts:

in a timing adjustment method for adjusting the timing of an event, there are the following steps:

a multiphase clock generating step for generating multiphase clocks, with said multiphase clocks composed of plural phase clocks of different phases that represent plural different timing adjustment quantities applied on said event,

and a multiphase clock use step in which any one said phase clock from said multiphase clocks is used, and an event change timing signal representing the changed timing of said event is generated.

11. A timing adjustment method of an event group characterized by the following facts:

the timing adjustment method for adjusting the timing of an event group composed of plural events has the following steps:

a step in which said event group is decomposed into individual events,

and a step in which the timing adjustment method described in Claim 10 is embodied for each of said decomposed events.

12. The timing adjustment method described in Claim 10 or 11 characterized by the following facts:

there is also a step in which an event timing signal representing said timing of events is generated; in this step, said event timing signal is in synchronization with said multiphase clocks.

13. The timing adjustment method described in Claim 10 or 11 characterized by the fact that it also has the fact that said multiphase clock generating step also contains

a step in which said multiphase clocks are generated in synchronization with a reference signal related to said events.

14. The timing adjustment method described in Claim 13 characterized by the fact that said multiphase clock is composed of plural phase clocks with equal spacing between them.

15. The timing adjustment method described in Claim 14 characterized by the fact that said phase clock has a clock portion representing the corresponding timing adjustment quantity.

16. The timing adjustment method described in Claim 14 characterized by the fact that said events are events on an optical disk recording medium.

17. The timing adjustment method described in Claim 15 characterized by the following facts: the events on said optical disk recording medium are rise events and fall events of the write pulses in the pulse width adjustment of the write pulses for writing on said optical disk recording medium;

said write pulses are for determining the timing of control of output of the laser used in write on said optical disk recording medium.

18. The timing adjustment method described in Claim 16 characterized by the fact that in said event timing signal generating step, said event timing signal is generated from said write pulses.

19. The timing adjustment method described in Claim 17 characterized by the fact that

there is also a step in which write pulses after a timing change are generated from said event change timing signal.

20. The timing adjustment method described in any of Claims 13-19 characterized by the fact that said multiphase clock generating step also contains

a step in which said reference signal related to said events is obtained from the wobble signal of said optical disk recording medium.

21. The timing adjustment method described in any of Claims 14-20 characterized by the fact that said optical disk recording medium has a rotation control system, such as a CAV system, zone CLV system, or CLV system.

22. The timing adjustment method described in Claim 14 characterized by the fact that said events are events in digital transmission data.

23. The timing adjustment method described in Claim 22 characterized by the fact that said multiphase clocks are generated from the transmission clock of said digital transmission data.

24. The timing adjustment method described in Claim 10 or 11 characterized by the fact that said multiphase clock use step also contains the following steps:

a step in which an adjustment quantity input that assigns the timing adjustment quantity applied on said events is received,

and a selection step in which one said phase clock having said timing adjustment quantity corresponding to said adjustment quantity input is selected as said event change timing signal.

25. The timing adjustment method described in Claim 24 characterized by the fact that said use step also contains

a step in which said event change timing signal is applied on said events.

26. The timing adjustment method described in Claim 10 or 11 characterized by the fact that said timing adjustment is performed by timing delay.

27. The timing adjustment method described in Claim 10 or 11 characterized by the fact that said plural different timing adjustment quantities are within a prescribed range.

28. A timing adjustment circuit characterized by the fact that a timing adjustment circuit for adjusting the timing of events is composed of the following means:

a multiphase clock generating means for generating multiphase clocks, with said multiphase clocks composed of plural phase clocks having different phases representing plural different adjustment quantities applied on said events,

and a multiphase clock use means that uses any one said phase clock selected from said multiphase clocks and generates an event change timing signal representing the changed timing of said events.

29. A timing adjustment circuit for an event group characterized by the fact that the timing adjustment circuit for an event group adjusts the timing of one event group composed of plural events, and it consists of the following means:

an event decomposition means that decomposes said event group into individual events,

and an event group timing adjustment means composed of timing adjustment circuits described in Claim 28 for said various events, respectively.

30. The timing adjustment circuit described in Claim 29 characterized by the fact that it contains a synthesis means that receives said event change timing signals generated by said timing adjustment circuits for said events in said event group and synthesizes them to generate a synthetic event change timing signal.

31. The timing adjustment circuit described in Claim 30 characterized by the fact that said timing adjustment circuits set for said events, respectively, contain a common multiphase clock generating means.

32. The timing adjustment circuit described in Claim 28 or 29 characterized by the fact that it also

contains a means for generating an event timing signal that represents timing of said events, with said event timing signal in synchronization with said multiphase clocks.

33. The timing adjustment circuit described in Claim 32 characterized by the fact that said timing adjustment is performed by means of timing delay.

34. The timing adjustment circuit described in Claim 32 characterized by the fact that said plural different timing adjustment quantities are within a prescribed range.

35. The timing adjustment circuit described in Claim 34 characterized by the fact that said multiphase clock use means contains an enlarging means that receives said event timing signal and, by delaying the event timing signal, enlarges said timing adjustment quantity by means of said multiphase clocks alone.

36. The timing adjustment circuit described in Claim 28 or 29 characterized by the fact that said multiphase clock generating means contains

a PLL circuit means that generates said multiphase clocks in synchronization with the reference signal pertaining to said events.

37. The timing adjustment circuit described in Claim 36 characterized by the fact that said events are events on an optical disk recording medium.

38. The timing adjustment circuit described in Claim 37 characterized by the following facts: said events on the optical disk recording medium are rise events and fall events of the write pulses for write on said optical disk recording medium in pulse width adjustment of said write pulses, and said write pulses are for determining the timing for control of output of a laser used in write on said optical disk recording medium.

39. The timing adjustment circuit described in Claim 38 characterized by the fact that said event timing signal generating means generates said event timing signal from said write pulses.

40. The timing adjustment circuit described in Claim 39 characterized by the fact that said multiphase clock use means also contains

a means for generating write pulses after a timing change from said event change timing signal.

41. The timing adjustment circuit described in any of Claims 36-40 characterized by the fact that

said multiphase clock generating means contains

a means for obtaining a reference signal pertaining to said events from the wobble signal of said optical disk recording medium.

42. The timing adjustment circuit described in Claim 41 characterized by the fact that said optical disk recording medium has a rotation control system, such as a CAV system, zone CLV system, or CLV system.

43. The timing adjustment circuit described in Claim 28 or 29 characterized by the fact that said multiphase clock use means contains the following means:

a means for receiving an adjustment quantity input that assigns the timing adjustment quantity applied on said events,

and a selection means that selects one said phase clock having said timing adjustment quantity corresponding to said adjustment quantity input as said event change timing signal from said multiphase clocks.

44. The timing adjustment circuit described in Claim 43 characterized by the fact that said multiphase clock use means also

contains an application means for applying said event change timing signal on said events.

45. A type of pulse width adjustment device for use in an optical disk recorder characterized by the fact that the pulse width adjusting device has a timing adjustment circuit described in any of Claims 28-44.

46. A type of optical disk recorder having a pulse width adjustment device described in Claim 45.

47. The optical disk recorder described in Claim 46 characterized by the fact that said optical disk recorder is a CD-R, CD-RW, DVD-R, DVD-RW, DVD+R, DVD+RW or DVD-RAM device.

48. A type of synchronization device having a timing adjustment circuit described in any of Claims 28-36, 43, and 44.